EPC C1 Gen2 UHF RFID IC
Fully-Passive Sensor Monitoring

Description

AS3211 is an EPC™ Class-1 Generation-2 compliant IC for UHF RFID applications. The chip offers advanced performance in sensor acquisition mode, due to an ultra-low power internal acquisition channel. It can be powered either by a battery or by the RF energy transmitted from a reader. In a Battery Assisted Passive (BAP) configuration, the AS3211 offers an increased reading range compared to passive RFID solutions.

AS3211 embeds 512 bits of low power non-volatile memory (EEPROM) that is organized in 4 banks as described in EPC Gen 2 standard. The chip supports the EPC data structure which is compliant with the EPC Global Tag Data Standards, Version 1.10, and is delivered with a Unique Identifier (UID) to ensure full traceability.

The chip integrates an acquisition channel including a 10-bit Analog to Digital Converter (ADC) to monitor an on-chip temperature sensor. It supports a temperature range from -40°C to +125°C.
Sensor data is available on demand by a reader using a simple read command in user memory as defined in EPC protocol. There is no need for any custom command.

AS3211 also provides digital interface for advanced applications such as machine to machine communication. It is made by a standard slave SPI and offers programmability and functionality setup. It also allows to trig data acquisition through the internal digital interface. Both the RF interface and the SPI bus provide the same functions.

Features

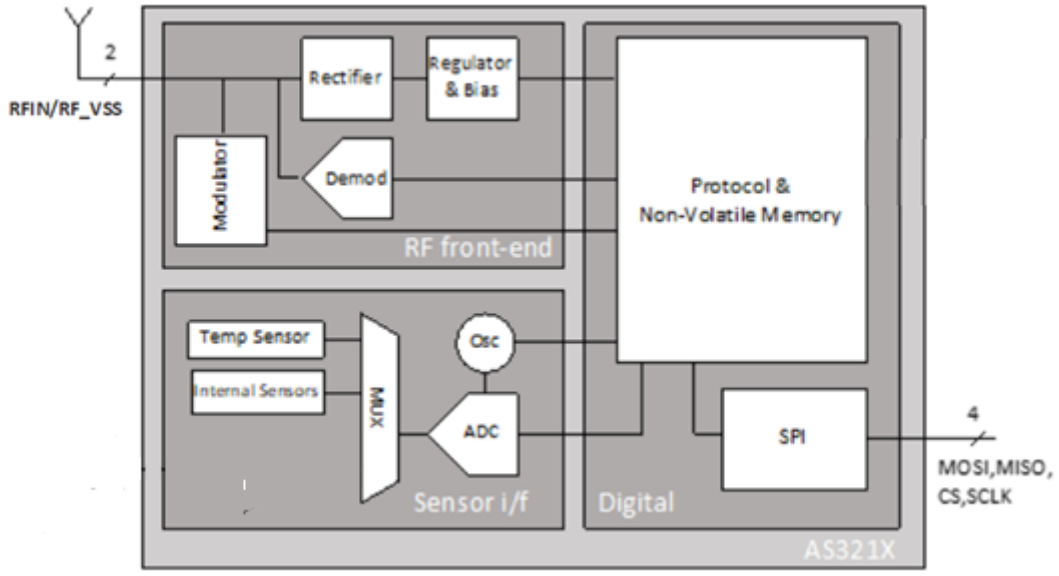
- ✓ EPC Gen2 compliant
- ✓ Fully passive applications
- ✓ 512-bit non-volatile memory (EEPROM)
- ✓ 48-bit manufacturer programmed IC Serial Number
- ✓ 192 bits for UII/EPC encoding
- ✓ 96 bits for User data
- ✓ Forward link data rates: 26.7 to 128 kbps assuming equiprobable data
- ✓ Return link data rates: 40 to 640 kbps with subcarrier modulated data rates of 0.625 to 320 kbps
- ✓ Integrated acquisition channel embedding a 10 bits ADC for temperature monitoring
- ✓ Integrated temperature sensor: -40°C to +125°C with typical accuracy of ±2°C over the full range
- ✓ Serial Peripheral Interface (SPI) Bus
- ✓ Battery assistance for increasing reading range
- ✓ Regulated power supply
- ✓ Extended operating temperature range: -40°C to +125°C

Applications

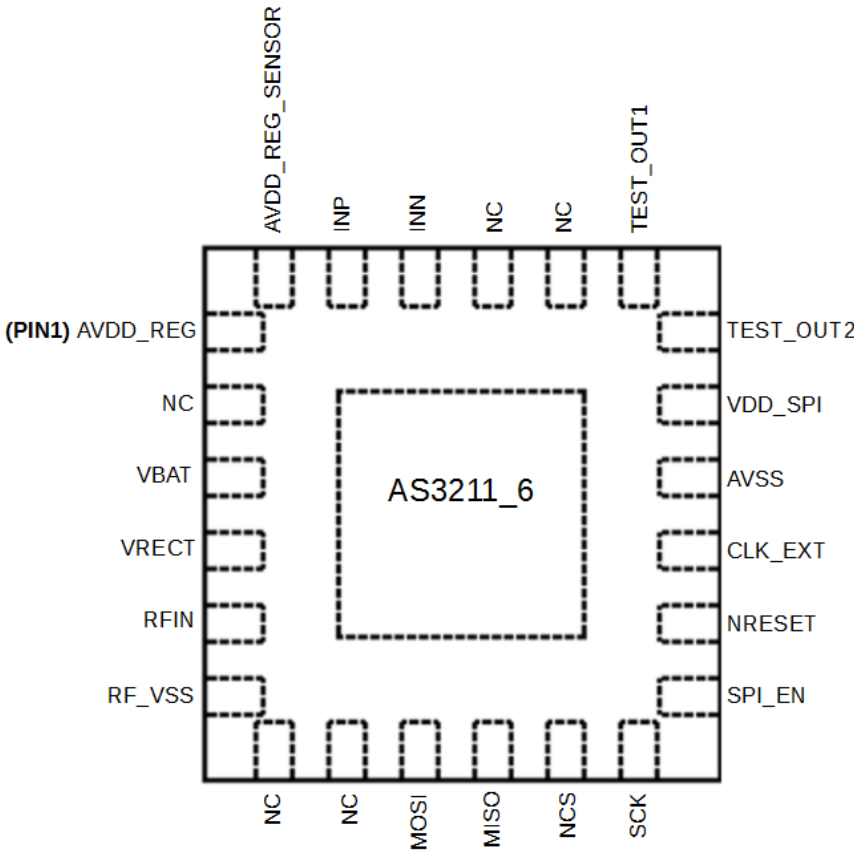
- ✓ Condition monitoring
- ✓ Supply chain management, tracking and tracing
- ✓ Cold chain monitoring

Table of Content

Block Diagram



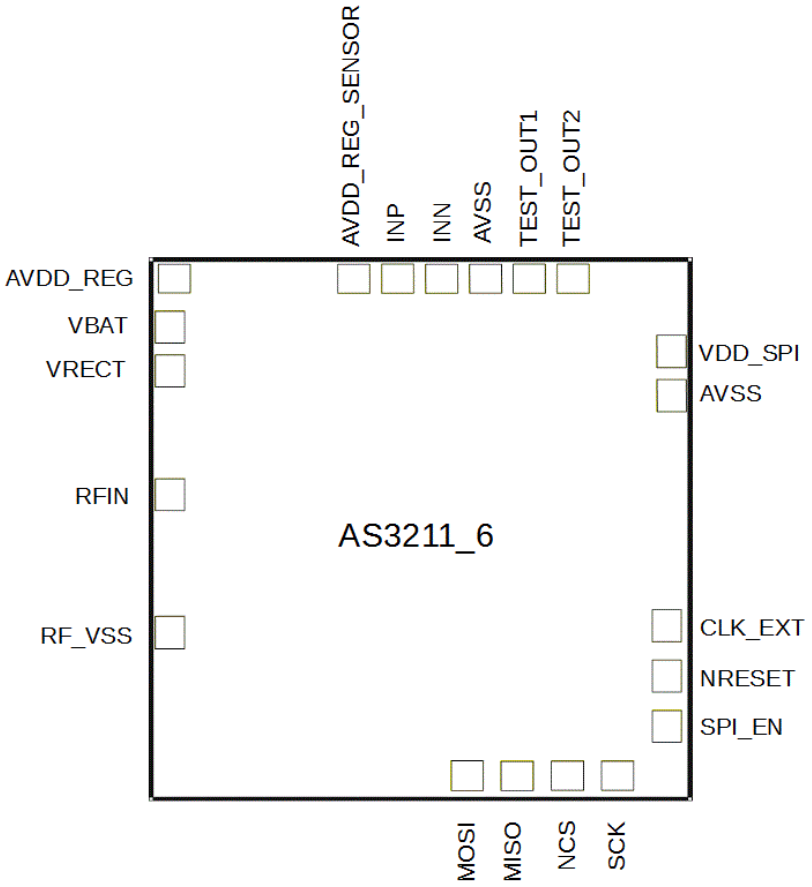
Pin Description : QFN24 4x4mm 0.5mm (Top View)



Pin	Name	Type	I/O	Description
1	AVDD_REG	A	O	1.0V Regulated Power Supply
2	NC	NA		Not Connected
3	VBAT	A	I	External Power Supply in BAP operation [1.8V;2.5V] (*) **Need to be connected to AVSS in passive operation**
4	VRECT	A	O	Non-Regulated Power Supply from RF field [1.2V;2.0V]
5	RFIN	RF	I	Antenna input
6	RF_VSS	A	I	For antenna connection) only (RF ground)
7	NC	NA		Not Connected
8	NC	NA		Not Connected
9	MOSI	D	I	1.8V SPI MOSI signal
10	MISO	D	O	1.8V SPI MISO signal
11	NCS	D	I	1.8V SPI Chip Select
12	SCK	D	I	1.8V SPI Clock signal
13	SPI_EN	D	I	1.8V SPI Enable signal
14	NRESET	D	I	1.8V external reset for digital part in SPI mode (SPI_EN=”1”)
15	CLK_EXT	D	I	External clock for digital part in SPI mode (SPI_EN=”1”)
16	AVSS	A	I	Ground of the IC
17	VDD_SPI	A	I	SPI 1.8V Power supply
18	TEST_OUT2	A	I/O	Analog test pin for input and output
19	TEST_OUT1	A	I/O	Analog test pin for input and output
20	NC	NA		Not Connected
21	NC	NA		Not Connected
22	INN	A	I	Not Used
23	INP	A	I	Not Used
24	AVDD_REG_SENSOR	A	O	Not Used

A: Analog, D: Digital (*) For write operation in the NVM, the power supply needs to be higher than 2.2V.

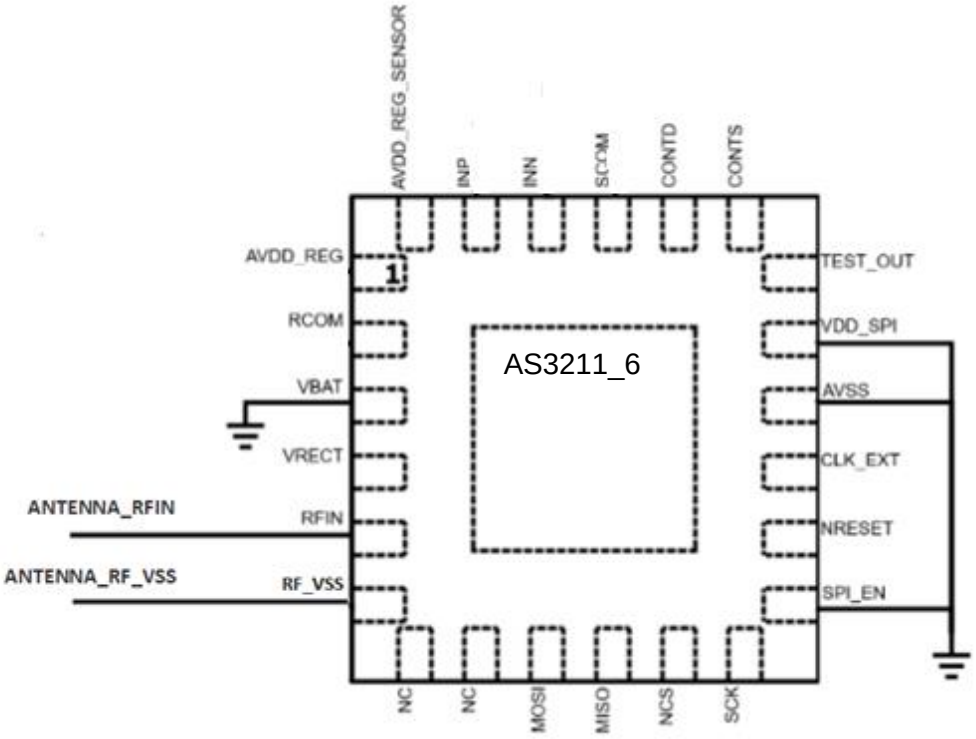
Pin Description : Bare Die 1.3mmx1.3mm (Top View)



DXF files are available upon request.

Typical Application

Temp sensor in passive operation.



In passive mode, the needed energy is provided by the RF field. The external power supply pin VBAT needs to be connected to AVSS to avoid active mode to turn on. It is recommended (not mandatory) to connect VDD_SPI to AVSS too, to avoid any unwanted activation of the SPI mode. By the same way, it is recommended to connect SPI_EN to AVSS, but this is not mandatory because it is pulled down internally. NRESET, CLK_EXT and the SPI inputs can be left floating (internal pull down too).

Application notes can be found on the following website: https://as321x.asygn.com/

Specification

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Tstorage	-50	150	°C
Voltage on all pads/pins except AVSS	Vpin	0	3.3	V
RF power into pad/pin RFIN	Pmax		15	dBm
Electrostatic discharge on all pads except RFIN	VESD	-1000	1000	V
Electrostatic discharge on RFIN	VESD_RF	-500	500	V

ESD are Human Body Model (HBM) values

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating temperature	Toperating	-40	+125	°C
Max RF power at RFIN	Pmax_op		15	dBm
RF carrier frequency	Fcarrier	860	960	MHz

Electrical Characteristics at 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Battery voltage for EEPROM read operation	Vread	0.9		3.3	V
Battery voltage for EEPROM power check, erase, and write operations	Vwrite	1.8		3.3	V
Average battery current in Sleep mode (No RF applied to the antenna)	Isleep		3.8		uA

RF Characteristics @25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Impedance	Zin_passive	Die form @ Pin=-10dBm Fcarrier = 866MHz Fcarrier = 915MHz		 7-j406 8.5-j383		 Ω Ω
		QFN24 @ Pin=-10dBm Fcarrier = 866MHz Fcarrier = 915MHz		 23-j213 30-j195		 Ω Ω
Write sensitivity in passive	Pwrite_passive			-12		dBm
Read sensitivity in passive	Pread_passive			-13		dBm
Read sensitivity in passive mode with temperature sensor	Pread_sensor			-13		dBm
Write sensitivity in BAP	Pwrite_bap	VBAT=2.2V		-16		dBm
Read sensitivity in BAP	Pread_bap	VBAT=2.2V		-16		dBm

NVM Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Erase / write endurance	Tcyc	Worst Case	10,000			Cycles
Retention	Tretention	T = 85°C	10			Years

I/O DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
MOSI, MISO, SCLK, NCS, SPI_EN, CLK_EXT, NRESET						
Input Low Voltage	VIL		0		0.3*VDD_SPI	V
Input High Voltage	VIH		0.7*VDD_SPI		VDD_SPI	V
Input pull-down	Rpulldown			100K		Ohm

Temperature Sensor Characteristics

NOTE: Toperating: -40°C to 125°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature Range	Trange		-40		125	°C
Resolution	Res			±0.35		°C
Accuracy after calibration	Acc	From -40°C up to 125°C		**±2 (*)**		°C
RF Sensitivity in passive mode operation for temperature sensor	Ptemp			-13		dBm

(*) ±2°C: this accuracy is obtained over the entire temperature range [-40°C / 125°C] after calibration at one point, i.e. at a single temperature.
This calibration is carried out during the production test of the wafers. The calibration temperature is the temperature of the test room (ambient temperature).

On request, if better accuracy is required, it can be achieved by:

1) reducing the t° range and performing the calibration at the central t° of this range,
2) using two calibration points (or more) instead of just one.

Functional Description

The AS3211 is mainly a passive UHF RFID IC which can be used in Battery Assisted Mode (BAP). It is compatible with all standard UHF RFID reader operating at 860MHz - 960MHz. It is powered either by a battery or by the RF field transmitted by the reader, which is received and rectified to generate a supply voltage for the device.

The AS3211 device is the first UHF RFID product embedding an integrated temperature sensor that provides an absolute temperature reading on demand.

Due to its full compatibility with EPC Gen 2 protocol, the IC is OFF most of the time. It only wakes up once an RF field is available with enough power to supply the chip. First operation performed is a start-up sequence loading all configuration words stored in NVM. The level of minimal power to operate is defined as sensitivity.

When a RF field is available with enough power to supply the chip, a power on reset (POR) signal rises and the tag wakes up. When the start-up or boot sequence is completed, the tag is ready to receive and demodulate commands from the interrogator.

In BAP mode, the tag wakes up as previously, when the RF field is available. The same sequence as above is performed.

Being compliant with EPC Global standards in UHF RFID applications, the maximum allowed time to perform the start-up sequence is 1.5ms. If permitted by the reader, it is however possible to increase by configuration the time allowed for the boot sequence to improve sensitivity. This feature is detailed later in register definition section.

A programmable 4-wire slave SPI bus is available for smart system integration. The SPI bus allows communications from a master SPI device and allows for control and data exchange between a reader and other components on a tag. All functionalities available from the RF reader are also available from the master SPI. The chip can be considered as symmetrical from a functional point of view. All NVM addresses and registers are available as absolute addresses (no banks) in SPI mode.

This device is in full compliance with ISO/IEC 18000-6 C, EPC™ Class-1 Generation-2, according to the following documents:

"ISO/IEC 18000-63 Information technology – Radio frequency identification for item management – Part 63: Parameters for air interface communications at 860 MHz to 960 MHz Type C”

"EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 Mhz - 960 MHz, Version 1.2.0” from EPCglobal Inc.

"EPCglobal Tag Data Standards, Version 1.10" from EPCglobal Inc.

EPC Optional Features supported

Optional Feature / Command	Supported	Comments
Kill Password	Yes	
Access Password	Yes	
Extended TID	No	Available upon request
User Memory	Yes	
Custom Commands	No	
Access Command	Yes	
Lock Command	Yes	
Kill Command	Yes	
BlockWrite Command	No	Available upon request
BlockErase Command	No	Available upon request
BlockPermalock Command	No	Available upon request
Error Specific Codes	TBD	
ASK and/or PSK Backscatter Modulation	Yes	Only ASK.
Recommissioning	No	
Battery Assisted Passive (BAP)	Yes	

Memory Map

The EEPROM is organized in four banks available for the user. The ISO/IEC 18000-6 type C and the EPC™ Class-1 Generation-2 specifications define four memory banks: Reserved, TID, UII/EPC, and User. The four memory banks are contiguous in EEPROM.

The EEPROM is divided as described in the following table:

Label			LogAddr	Bank
USER7	0x	7	7	USER
USER6	0x	6	6	
USER5	0x	5	5	
USER4	0x	4	4	
USER3	0x	3	3	
USER2	0x	2	2	
ACQ_TEMP	0x	1	1	
ACQ_SENS	0x	0	0	
TRIM0	0x	7	7	TID
RN16 SEED	0x	6	6	
SN0	0x	5	5	
SN1	0x	4	4	
SN2	0x	3	3	
XTID HEADER	0x	2	2	
MDID+TMN	0x	1	1	
MDID+TMN	0x	0	0	
RFU	0x	10	16	EPC
CONFIG1	0x	F	15	
CONFIG0	0x	E	14	
EPC0	0x	D	13	
EPC1	0x	C	12	
EPC2	0x	B	11	
EPC3	0x	A	10	
EPC4	0x	9	9	
EPC5	0x	8	8	
EPC6	0x	7	7	
EPC7	0x	6	6	
EPC8	0x	5	5	
EPC9	0x	4	4	
EPC10	0x	3	3	
EPC11	0x	2	2	
STORED_PC	0x	1	1	
STORED_CRC	0x	0	0	
ACCESS_PASSWD0	0x	3	3	RESERVED
ACCESS_PASSWD1	0x	2	2	
KILL_PASSWD0	0x	1	1	
KILL_PASSWD1	0x	0	0	

Configuration Definition

In this section, all configuration and trim bits are defined. They are mainly controlling some parameters of the acquisition channel.

Trim and configuration words are read from memory during the tag boot sequence and written in registers. Changing Configuration and trim words in memory then only takes effect on next power up.

Config0 - EPC bank address 0xE (14)

Bit	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Name	RFU		RFU	RFU	RFU	RFU	CH_DLY		BRIDGE_LEN		SCA_CLK_CYCLES		IA_GAIN		IA_EARLY_EN	ADC_REF

All bits in CONFIG0 are defined and explained in the table below.

Some setting bits (in grey) do not have to be changed. They were meant to evaluation by Asygn engineering team.

Name	Description
RFU	Reserved for future use
CH_DLY<1:0>	Storage capacitance charge time : Increase boot-sequence duration to optimize charging of storage capacitance. Allow to increase sensitivity if EPC start-up time is permitted by reader. ‘00’: 50us (Default) ‘01’: 200us ‘10’: 400us ‘11’: 800us
BRIDGE_LEN<1:0>	Has to be set to ‘00’
SCA_CLK_CYCLES<1:0>	Has to be set to ‘00’
IA_GAIN<1:0>	Has to be set to ‘00’
IA_EARLY_EN	Has to be set to “0”
ADC_REF	ADC input range ‘0’: Reference are 0 and AVDD_REG=1.0V. ADC Input dynamic is 2V ‘1’: Reference are 0.25xAVDD_REG and 0.75. ADC Input dynamic is 1V Recommended value = ‘0’

Config1 - EPC bank address 0xF (15)

Bit	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Name	RFU		TS_MODE		SENSOR_SELECT				IA_FSMPL		ADC_TSMPL		ADC_FSMPL		ADC_NSMPL	

All bits in CONFIG1 are defined and explained in the table below.

Some setting bits (in grey) do not have to be changed. They were meant to evaluation by Asygn engineering team.

Name	Description
RFU	Reserved for future use
TS_MODE<1:0>	Has to be set to '10'
SENSOR_SELECT<3:0>	'1000': Temperature sensor 'Others': Not available
IA_FSMPL<1:0>	Has to be set to '00'
ADC_TSMPL<1:0>	Has to be set to '11'
ADC_FSMPL<1:0>	Has to be set to '00'
ADC_NSMPL<1:0>	Number of samples converted in a row, for averaging. Data format is presented in the SENSOR_DATA section. '00': Only one conversion is performed '01': 2 conversions '10': 4 conversions '11': 8 conversions

Temperature Data

Temperature data is stored in a register at user memory address 1. It is accessible thanks to a simple Read command from the reader. Data acquired is presented as shown below depending on the value of the ADC_NSMPL used for averaging. All samples taken are added and written in the register as well as the “powerok” indicator and the number of samples. In this way the interrogator can perform averaging in the way wanted by the application.

PWR_OK is a status bit indicating that the power supply stayed into the wanted range during measurement ensuring accuracy and precision of the measurement within specification.

	NSMPL	PWR_OK	ACQ_SENS / ACQ_TEMP DATA												
# of samples	15:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	NSMPL	PWR_OK				D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	NSMPL	PWR_OK			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0,	D-1
4	NSMPL	PWR_OK		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0,	D-1	D-2
8	NSMPL	PWR_OK	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D-1	D-2	D-3

SPI Interface

The SPI interface gives access to memory and registers, that is :

- EEPROM physical memory,
- Configuration and Trim registers,
- Sensor data registers (read-only),
- MDID, XTID_HEADER, STORED_CRC (read-only).

SPI gets the priority vs RF communication as soon as SPI-EN is set high.

Lock status programmed through EPC lock commands is ignored by SPI, as well as the tag status. All memory locations and registers are accessible, even when the tag is killed.

SPI Mode

The SPI_EN pad, when tied to 1, enables the SPI interface. In SPI mode, the clock and reset of the chip's digital part must be provided through CLK_EXT and NRESET pads.

CLK_EXT rate must be set to 2.56 MHz. NRESET must be asserted low to properly reset the chip.

The SPI mode invalidates the use of the RF reader.

SPI_EN	Description
0	SPI interface is disabled RF reader is enabled Clock and reset are provided by internal oscillator and on-chip POR.
1	SPI interface is enabled RF reader is disabled Clock and reset are provided by CLK_EXT and NRESET

SPI Bus

The SPI interface is the standard 4-wire interface:

SPI interface	Description	Pin direction	Comments
MISO	Slave Data Output	Output	Driven low in RF mode Tri-stated in SPI mode when NCS=1
MOSI	Slave Data Input	Input	Pad pull down always activated
NCS	Chip Select	Input	Active low. Pad pull down always activated
SCK	Serial Clock	Input	Pad pull down always activated

- NCS : device selection. The device is selected when NCS is low. When unused, the NCS pad is pulled down.
- SCK : Serial clock. The Serial Clock is driven by the External Master SPI. Due to internal resynchronization, the SCK rate must be less than 128kHz.

SCK frequency < 128kHz

MOSI : Slave Data input. When unused, a pull-down keeps the signal at 0.
MISO : Slave Data Output. When unused in SPI mode, the output is set High Z.

SPI register map

REGISTER	ADDR	RD/WR
TEST_REG	16'h0000	RD/WR
STORED_CRC_REG	16'h0001	RD ONLY
MDID_MSB_REG	16'h0002	RD ONLY
MDID_LSB_REG	16'h0003	RD ONLY
XTID_HEADER_REG	16'h0004	RD ONLY
SENS_REG	16'h0005	RD ONLY
TEMP_REG	16'h0006	RD ONLY
TRIM0_REG	16'h0007	RD/WR
CONFIG0_REG	16'h0008	RD/WR
CONFIG1_REG	16'h0009	RD/WR
CONFIG2_REG	16'h000A	RD/WR

Access to registers are done using the READ_REG and WRITE_REG commands (See section on SPI commands) and the above register map.

The TEST_REG register drives the AFE test mode and the NVM Test pins (Refer to Test section). TEST_REG = 16'h0000 selects the normal functional mode. This is the default value of the TEST_REG register on power up.

Bit 15 of TEST_REG register, when set, is used to trig a new acquisition.

The address field of TEST_REG register is 0x00. This register is not included in the EPC memory map and can be written via the WRITE_REG instruction only.

SPI Commands

SPI available commands are:

Instruction	Description	Instruction code	Comments	Frame length
RDSR	Read Status Register	0x00000101	Returns the 8-bit status register	8 + 8 bits
WRITE	Write to memory array	0x00000010	Writes a 16-bit word in memory array	8 + 8 + 16 bits
READ	Read to memory array	0x00000011	Reads a 16-bit word in memory array	8 + 8 + 16 bits
WRITE_REG	Write to Registers	0x10000010	Writes a 16-bit word in register	8 + 8 + 16 bits
READ_REG	Read to Registers	0x10000011	Reads a 16-bit word from register	8 + 8 + 16 bits

Available commands are listed above. If an invalid code command is received, the device automatically enters a Wait State until it is deselected (NCS high). Command code is 8-bit length. Addresses are 8-bit length, data are always 16-bit.

Commands available are detailed below.

WRITE

WRITE can be performed only if a WRITE is not already in progress in memory. Once the 8 bits of the WRITE command have been sent, the SPI device waits for address and data. They are shifted-in, MSB first. After this sequence, the device enters a wait state, waiting for the chip select to be driven high. The WRITE is interrupted if the NCS line is deselected during data or address transfer.

READ

READ can be performed if a WRITE is not in progress. Once the 8 bits of the READ command have been sent, the device waits for an 8-bit address. Address is shifted-in MSB first. Data is shifted-out MSB first. The READ is interrupted if the NCS line is deselected during the transfer.

RDSR

RDSR returns the Status Register value. This instruction can also be executed if a memory WRITE is in progress and is specially intended to report the end of the write. Once the 8 bits of the RDSR command have been sent, the 8-bit Status register is shifted-out, MSB first.

The RDSR returns the WREN value, and the status of the WRITE in Progress (WIP).

	7	6	5	4	3	2	1	0
RDSR	RFU							WIP

WIP: 1: Write is in Progress, 0: No write in progress

The READ is interrupted if the NCS line is deselected during the transfer.

WRITE_REG

The WRITE_REG enables the SPI to directly access the CONFIG0 to CONFIG1, TRIM0 and TEST registers in write mode. Writing configuration and trim registers using WRITE_REG instruction takes immediate effect. At the opposite, writing configuration and trim using WRITE instruction has no immediate impact since new values are written into memory. These changes will be effective on next power up after these data will be downloaded from memory into registers.

Addresses of registers using the WRITE_REG command are listed below.

READ_REG

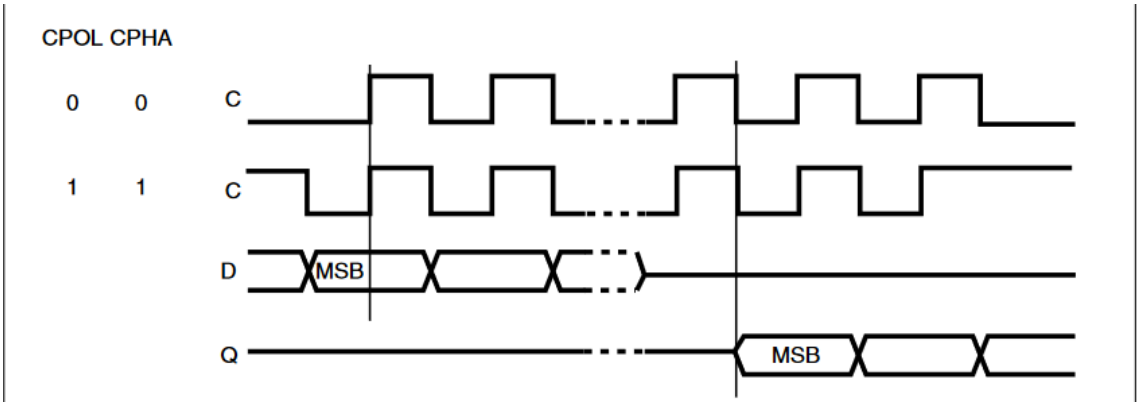
The READ_REG enables the SPI to directly access the above registers in read mode. All registers are readable.

SPI Protocol

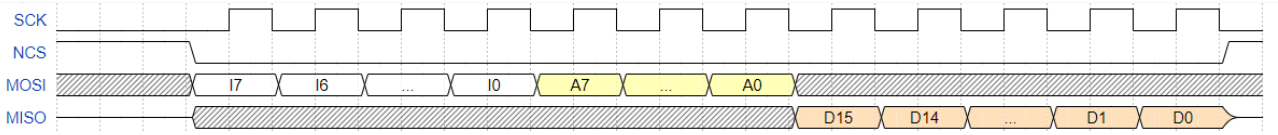
The SPI device performs 8-bit transfers, MSB first. It can be driven by any master device running in the following modes:

CPOL=0, CPHA=0,
CPOL=1, CPHA=1.

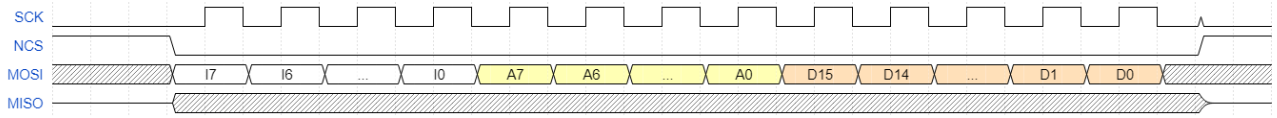
For these 2 modes, input data on MOSI is latched in on the rising edge of SCK and output data (MISO) is available from the falling edge of clock, as shown below.



SPI frames have length multiples of 8 bits.

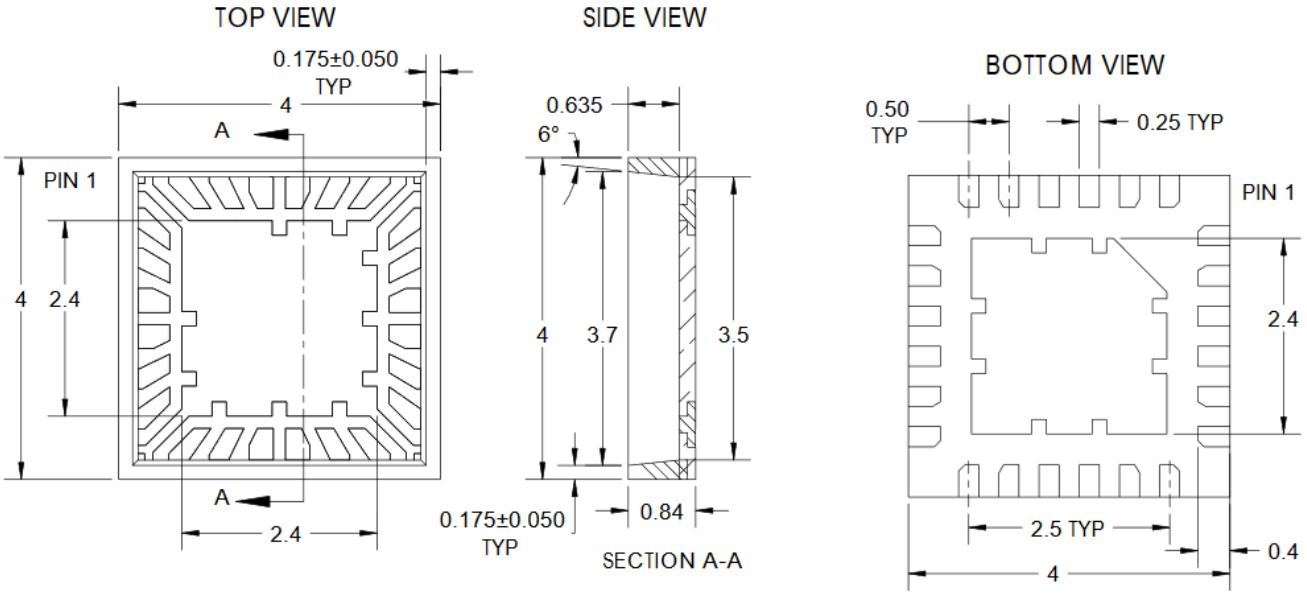


READ sequence : 32-bit frame



WRITE sequence or WRITE_REG sequence : 32-bit frame

Package information

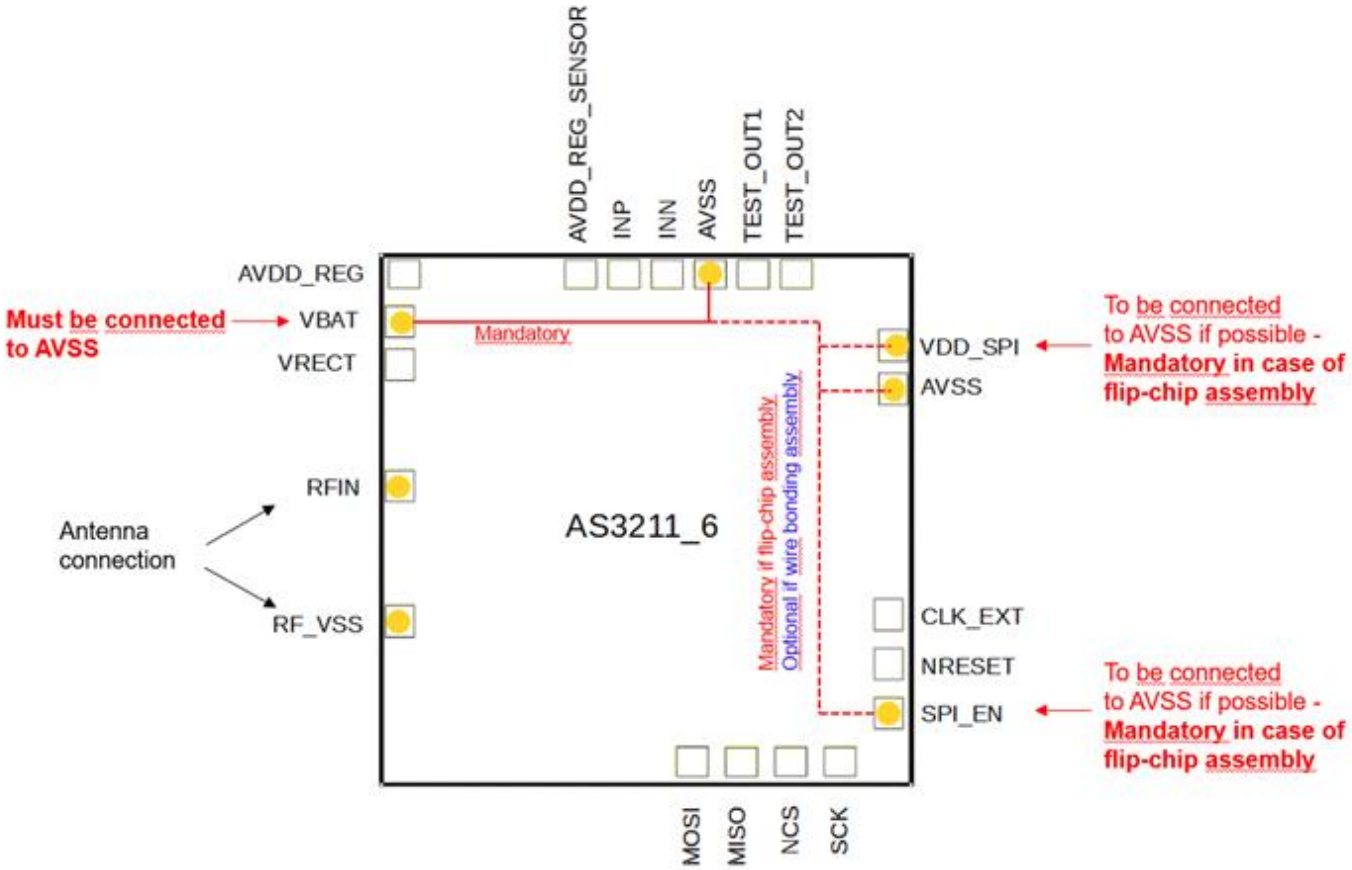


Bare Dies Information

Bumps (DXF available on demand)

Main information concerning bumps are listed below:

- Wafer Thickness : 250µm
- Pads size:70x77µm²
- Passivation opening: 70µmx77µm
- Bumps type: Accu bumps (Au)
- Bumps thickness: 45µm
- Bumps diameter: 80µm



Product Support

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